What is claimed is:

1. A duty cycle correction circuit of a delay locked loop, comprising:

a differential amplifier, which receives and amplifies differential reference clock signals through a first input terminal and a second input terminal, and outputs differential output signals to a first differential output terminal and a second differential output terminal, respectively;

a first transmission circuit, which is connected between the first differential output terminal and a first node, and transmits a signal of the first differential output terminal to the first node, in response to transmission control signals;

a second transmission circuit, which is connected between the second differential output terminal and a second node, and transmits a signal of the second differential output terminal to the second node, in response to the transmission control signals;

a first storage unit, which is connected between the first node and a ground voltage and accumulates electric charges on the first node;

a second storage unit, which is connected between the second node and the ground voltage and accumulates electric charges on the second node; and

a current control circuit, which controls an amount of electric charges accumulated in the first storage unit and an amount of electric charges accumulated in the second storage unit, in response to a corresponding switching control signal.

2. The duty cycle correction circuit of claim 1, wherein each of the first transmission circuit and the second transmission circuit is a transmission gate.

3. The duty cycle correction circuit of claim 1, wherein each of the first storage unit and the second storage unit is a MOS transistor.

4. A delay locked loop comprising:

a DLL core, which receives an external clock signal and generates an internal clock signal synchronized to the external clock signal;

a buffer, which buffers the internal clock signal and outputs differential reference clock signals; and

a duty cycle correction circuit, which generates duty rate control signals each having a predetermined offset corresponding to a difference of respective duty cycles of the differential reference clock signals; and

a control signal generation circuit, which generates switching control signals for controlling the offset, and outputs the switching control signals to the duty cycle correction circuit,

wherein the DLL core corrects a duty cycle of the internal clock signal, in response to the duty rate control signals.

5. The delay locked loop of claim 4, wherein the duty cycle correction circuit comprises:

a differential amplifier, which receives and amplifies the differential reference clock signals through a first input terminal and a second input terminal, and outputs differential output signals to a first differential output terminal and a second differential output terminal, respectively;

a first transmission circuit, which is connected between the first differential output terminal and a first node, and transmits a signal of the first differential output terminal to the first node, in response to transmission control signals;

a second transmission circuit, which is connected between the second differential output terminal and a second node, and transmits a signal of the second differential output terminal to the second node, in response to the transmission control signals;

a first storage unit, which is connected between the first node and a ground voltage and accumulates electric charges on the first node;

a second storage unit, which is connected between the second node and the ground voltage and accumulates electric charges on the second node; and

a control circuit, which controls an amount of electric charges accumulated in the first storage unit and an amount of electric charges accumulated in the second storage unit, in response to corresponding switching control signals.